IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An electronic system comprising:

a processor, which generates and sends one or more memory access requests; and

multiple memory modules, operatively coupled together through a communications bus, which return data requested in the one or more memory access requests, wherein each of the multiple memory modules is a data source, and a memory module of the multiple memory modules

determines that first source data and second source data are available,

generates a header for at least one of the first source data and the second source data,

allocates one or more first contiguous lanes within a first section of a data block to at least some of the first source data, wherein the data block comprises a set of multiple lanes, and each lane includes a set of configurable bits,

allocates one or more second contiguous lanes within a second section of the data block to at least some of the second source data, wherein the second section begins at a next lane, which is contiguous with the first section, and

sends, over the communications bus and during a data block transmission period, the at least a portion of the first source data within the first section of the data block, and the at least a portion of the second source data within the second section of the data block, wherein the header is positioned between the at least some of the first source data and the at least some of the second source data.

2. (Original) The electronic system of claim 1, further comprising:

a link controller, operatively coupled between the processor and to at least one of the multiple memory modules, which receives the one or more memory access requests, and generates and sends one or more memory access commands, based on the one or more memory access requests, to the multiple memory modules over the communications bus.

3. (Original) The electronic system of claim 2, further comprising:

the communications bus, wherein a memory module receives data from one or more other memory modules from a downstream direction on a first part of the communications bus, and the memory module sends the at least a portion of the first source data and the at least a portion of the second source data toward the link controller on a second part of the communications bus.

4. (Original) The electronic system of claim 1, wherein a memory module comprises:

means for receiving downstream data from a second memory module over the communications bus, wherein the downstream data is the first source data;

means for receiving local data from one or more memory storage units accessible to the memory module, wherein the local data is the second source data; and

means for assembling the downstream data and the local data into the data block.

5. (Original) The electronic system of claim 1, wherein a memory module comprises:

means for receiving downstream data from a second memory module over the communications bus, wherein the downstream data is the second source data;

means for receiving local data from one or more memory storage units accessible to the memory module, wherein the local data is the first source data; and

means for assembling the downstream data and the local data into the data block.

6. (Original) The electronic system of claim 1, wherein the electronic system is a computer.

7. (Currently Amended) A memory module comprising:

one or more memory storage units for storing local data; and

a hub, operatively coupled to the one or more memory storage units and to a communications bus over which the hub can receive downstream data from one or more other hubs, wherein the hub

determines that first source data and second source data are available,

generates a header for at least one of the first source data and the second source data,

allocates one or more first contiguous lanes within a first section of a data block to at least some of the first source data, wherein the data block comprises a set of multiple lanes, and each lane includes a set of configurable bits,

allocates one or more second contiguous lanes within a second section of the data block to at least some of the second source data, wherein the second section begins at a next lane, which is contiguous with the first section, and

sends, over the communications bus and during a data block transmission period, the at least a portion of the first source data within the first section of the data block, and the at least a portion of the second source data within the second section of the data block, wherein the header is positioned between the at least a portion of the first source data and the at least a portion of the second source data.

8. (Original) The memory module of claim 7, wherein the one or more memory storage units and the hub are co-located on a single substrate that is removably connectable to the communications bus.

9. (Original) The memory module of claim 7, wherein the one or more memory storage units includes one or more random access memory components.

10. (Original) The memory module of claim 9, wherein the one or more random access memory components includes one or more dynamic read only memory components.

11. (Original) The memory module of claim 7, wherein the one or more memory storage units includes one or more read only memory components.

12. (Original) The memory module of claim 7, wherein the hub includes one or more application specific integrated circuits.

13. (Original) The memory module of claim 7, wherein the hub comprises:

means for receiving the downstream data from a second hub over the communications bus, wherein the downstream data is the first source data;

means for receiving the local data from the one or more memory storage units, wherein the local data is the second source data; and

means for assembling the downstream data and the local data into the data block.

14. (Original) The memory module of claim 7, wherein the hub comprises:

means for receiving the downstream data from a second hub over the communications bus, wherein the downstream data is the second source data;

means for receiving the local data from the one or more memory storage units, wherein the local data is the first source data; and

means for assembling the downstream data and the local data into the data block.

15. (Previously Presented) An apparatus for assembling and sending data comprising:

means for receiving local data from one or more memory storage units;

means for receiving downstream data over a communications bus from one or more downstream data sources; and

means for making a determination of how the local data and the downstream data will be sent over the communications bus, wherein making the determination includes

allocating one or more first contiguous lanes within a first section of a data block to at least some of the local data, wherein the data block comprises a set of multiple lanes, and each lane includes a set of configurable bits,

allocating one or more second contiguous lanes within a second section of the data block to at least some of the downstream data, wherein the first section and the second section are contiguous, and

positioning a header portion between the first section and the second section.

16. (Original) The apparatus of claim 15, further comprising:

means for generating a first access request to send the local data over the communications bus; and

means for generating a second access request to send the downstream data over the communications bus,

wherein the means for making the determination receives the first access request and the second access request, and bases the determination on the first access request and the second access request.

17. (Original) The apparatus of claim 15, further comprising:

means for arranging the local data and the downstream data into the data block, according to the determination; and

means for sending the data within the data block over the communications bus during a data block transmission period.

18. (Currently Amended) An apparatus for sending data over a communications bus, the apparatus comprising:

means for receiving first source data from a first data source;

means for receiving second source data from a second data source; and

means for sending the first source data and the second source data over the communications bus, wherein sending the first source data and the second source data includes

providing a first header for ~~at least one of~~ the first source data and a second header for the second source data,

sending the first source data and the first header over the communications bus,

identifying a first breakpoint corresponding to an end of the first source data,

sending the second source data and the second header over the communications bus, wherein the second header is positioned contiguously with the end of the first source data, and

identifying a second breakpoint corresponding to an end of the second source data.

19. (Original) The apparatus of claim 18, wherein the means for receiving the first source data includes means for receiving downstream data from the communications bus, and the means for receiving the second source data includes means for receiving local data from one or more local memory storage units.

20. (Original) The apparatus of claim 18, wherein sending the first source data over the communications bus includes:

arranging a first portion of the first source data within a data block structure during a first processing period, wherein the data block structure includes a fixed number of contiguous, configurable bits; and

arranging a remainder portion of the first source data within a first section of the data block structure during a second processing period, wherein the first section includes a first set of contiguous bits.

21. (Original) The apparatus of claim 20, wherein identifying the first breakpoint includes:

identifying the first breakpoint as an end of the first section of the data block structure during the second processing period.

22. (Original) The apparatus of claim 21, wherein sending the second source data over the communications bus includes:

arranging a first portion of the second source data within a second section of the data block structure during the second processing period, wherein the second section is contiguous with the first section, and the second section includes a second set of contiguous bits.

23. (Original) The method of claim 22, wherein the data block structure includes a fixed number of lanes, each lane includes a same number of bits, the first section of the data block structure includes a first set of the fixed number of lanes, and the second section of the data block structure includes a second set of the fixed number of lanes.

24. (Currently Amended) A method for sending data on a communications bus, the method comprising:

arranging a first portion of first source data within a data block structure during a first processing period, wherein the data block structure includes a fixed number of contiguous, configurable bits and further wherein the first portion of the first source data includes a first header portion;

sending the first portion of the first source data over the communications bus;

arranging a remainder portion of the first source data within a first section of the data block structure during a second processing period, wherein the first section includes a first set of contiguous bits;

arranging a first portion of second source data within a second section of the data block structure during the second processing period, wherein the second section is contiguous with the first section, and the second section includes a second set of contiguous bits, wherein the first portion of the second source data includes a second header portion that is positioned between the first section and the second section; and

sending the remainder portion of the first source data and the first portion of the second source data over the communications bus.

25. (Original) The method of claim 24, further comprising:

making an indication, during the first processing period, that a breakpoint in the first source data will occur during the second processing period.

26. (Original) The method of claim 24, further comprising:

making an indication, during the first processing period, of a location of an end of the first section.

27. (Original) The method of claim 24, wherein the data block structure includes a fixed number of lanes, each lane includes a same number of bits, the first section of the data block structure includes a first set of the fixed number of lanes, and the second section of the data block structure includes a second set of the fixed number of lanes.

28. (Original) The method of claim 27, further comprising:

making an indication, during the first processing period, of a lane identifier that corresponds with a last lane of the first section.

29. (Original) The method of claim 27, further comprising:

making an indication, during the first processing period, of a lane identifier that corresponds with a first lane of the second section.

30. (Original) A computer-readable medium having computer-executable instructions for performing the steps recited in claim 24.

31. (Currently Amended) A method comprising:

determining that first source data and second source data are available;

generating [[a]] at least one header ~~for at least one of the first source data and the second source data~~;

allocating one or more first contiguous lanes within a first section of a data block to at least some of the first source data, wherein the data block comprises a set of multiple lanes, and each lane includes a set of configurable bits;

allocating one or more second contiguous lanes within a second section of the data block to at least some of the second source data, wherein the second section begins at a next lane, which is contiguous with the first section; and

sending, over a communications bus and during a data block transmission period, the at least a portion of the first source data within the first section of the data block, and the at least a portion of the second source data within the second section of the data block, wherein the header is positioned between the at least some of the first source data and the at least some of the second source data.

32. (Original) The method of claim 31, wherein determining that the first source data and the second source data are available comprises:

receiving a first indicator that the first source data is available from a first data source; and

receiving a second indicator that the second source data is available from a second data source.

33. (Original) The method of claim 31, wherein determining that the first source data and the second source data are available comprises:

receiving a first request to send the first source data over the communications bus; and

receiving a second request to send the second source data over the communications bus.

34. (Original) The method of claim 31, wherein allocating the one or more second contiguous lanes comprises:

receiving information that enables an identification of which lane is the next, contiguous lane; and

allocating a number of lanes to the at least some of the second source data, wherein a first lane of the number of lanes is the next, contiguous lane.

35. (Original) A computer-readable medium having computer-executable instructions for performing the steps recited in claim 31.

36. (Previously Presented) A method comprising:

arranging first source data from a first source within a first section of a data block structure, wherein the first source data includes a first header portion, and wherein the data block structure includes a fixed number of contiguous, configurable bits, and data within the data block structure is periodically sent out on a communications bus;

determining that second source data from a second source is available to be sent over the communications bus, wherein the second source data includes a second header portion;

requesting access to the communications bus to send the second source data;

receiving an indication of where, within the data block structure, at least a portion of the second source data should be placed;

arranging the at least a portion of the second source data within the data block structure according to the indication, resulting in the at least a portion of the second source data occupying a second section of the data block that is contiguous with an end of the first section, wherein the second header portion is positioned between the second section and the end of the first section; and

sending the first source data and the at least a portion of the second source data over the communications bus during a data block transmission period.

37. (Original) The method of claim 36, wherein the data block structure includes a fixed number of lanes, each lane includes a same number of bits, the first section of the data block structure includes a first set of the fixed number of lanes, and the second section of the data block structure includes a second set of the fixed number of lanes.

38. (Original) The method of claim 37, wherein receiving the indication comprises receiving a lane identifier that corresponds with a last lane of the first section.

39. (Original) The method of claim 37, wherein receiving the indication comprises receiving a lane identifier that corresponds with a first lane of the second section.

40. (Original) The method of claim 37, further comprising:

predicting where a breakpoint will occur in the second source data.

41. (Original) A computer-readable medium having computer-executable instructions for performing the steps recited in claim 36.

42. (Previously Presented) A method comprising:

arranging first source data within a first section of a data block structure, wherein the first source data includes a first header portion, and wherein the data block structure includes fixed number of contiguous, configurable bits;

receiving a request to send second source data over a communications bus, wherein the second source data includes a second header portion;

identifying a location of a breakpoint in the first source data;

arranging at least a portion of the second source data within a second section of the data block structure after the breakpoint, wherein the second section is contiguous with an end of the first section; and

sending the first source data and the at least a portion of the second source data over the communications bus during a data block transmission period.

43. (Original) The method of claim 42, wherein the data block structure includes a fixed number of lanes, each lane includes a same number of bits, the first section of the data block structure includes a first set of the fixed number of lanes, and the second section of the data block structure includes a second set of the fixed number of lanes.

44. (Original) The method of claim 43, wherein identifying the location comprises identifying a lane that corresponds with a last lane of the first section.

45. (Original) The method of claim 43, wherein identifying the location comprises identifying a lane that corresponds with a first lane of the second section.

46. (Original) A computer-readable medium having computer-executable instructions for performing the steps recited in claim 42.